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| **No.** | **List of Lab Experiments** |
| **1** | Implementation of Basic Gates and Universal Gates. |
| **2** | Implementation of Half Adder using  basic gates. |
| **3** | Implementation of Half Subtractor using basic gates. |
| **4** | Simplify equation and implement the simplified ckt. |
| **5** | Implementation of Binary to Excess-3 code conversion for 4 variable I/P. |
| **6** | Implementation of binary Parallel Adder using IC 74283. |
| **7** | Design Full Adder using Decoder |
| **8** | Implementation of boolean Functions using MUX. |
| **9** | Implement J-K F/F using NAND gate. |

**Course Code:** CSE 206

**Course Title:** Digital logic design Lab

**Submitted to:**

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**Submitted by:**

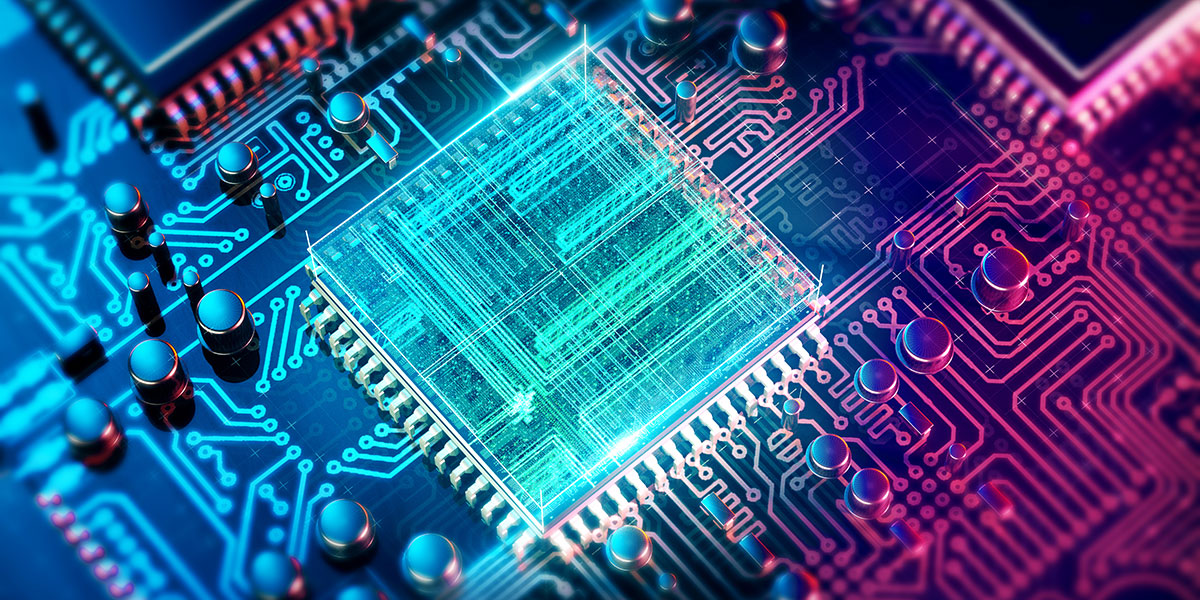
Name:

ID:

Intake: 39 Section: 1

Program: B.Sc. in CSE

Semester: Fall 19-20



Date of Submission: 12.01.2020

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